WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor chip having a semiconductor element and a plurality of electrodes;

a die pad smaller than a main surface of the semiconductor chip and bonded to a back side of the semiconductor chip;

a sealing member which seals the semiconductor chip with resin;

a plurality of leads each comprising an outer terminal portion exposed to a mounting surface of the sealing member and an inner lead portion positioned inside the sealing member; and

a plurality of bonding wires which connect the plural electrodes of the semiconductor chip and the plural inner lead portions with each other electrically,

wherein the inner lead portions of the plural leads are each bent in a direction away from the mounting surface of the sealing member.

2. A semiconductor device according to claim 1,

wherein the semiconductor chip comprises:

a first wiring formed on a semiconductor substrate and connected electrically to a ground potential;

a first insulating film formed on the first wiring;

and

a second wiring formed on the first insulating film and serving as a signal transmission line,

the second wiring including a first region, a second region, and a third region,

the second region of the second wiring being positioned between the first region and the third region,

with bonding wires being connected to the first region of the second wiring, and

the width of the second wiring in the second region being larger than the width thereof in the third region.

3. A semiconductor device according to claim 1, wherein the die pad is exposed to a surface opposite to the mounting surface of the sealing member.

4. A semiconductor device according to claim 3, wherein a heat sink is attached to the exposed portion of the die pad.

5. A semiconductor device according to claim 1, wherein the bonding wires are each 0.65 mm or less in length.

6. A semiconductor device comprising:

a semiconductor chip having a semiconductor element and a plurality of electrodes;

a die pad smaller than a main surface of the semiconductor chip and bonded to a back side of the semiconductor chip;

a sealing member which seals the semiconductor chip with resin;

a plurality of leads each comprising an outer terminal portion exposed to the exterior of the sealing member and an inner lead portion positioned inside the sealing member, at least one of each said outer terminal portion and each said inner lead portion having a portion bent in a direction away from a surface on which the outer terminal portions of the plural leads are arranged; and

a plurality of bonding wires which connect the plural electrodes of the semiconductor chip and the plural inner lead portions with each other electrically,

the semiconductor chip comprising:

a first wiring formed on a semiconductor substrate and connected electrically to a ground potential;

a first insulating film formed on the first wiring; and

a second wiring formed on the first insulating film and serving as a signal transmission line,

the second wiring including a first region, a second region, and a third region,

the second region of the second wiring being positioned between the first region and the third region,

with bonding wires being connected to the first

region of the second wiring, and

the width of the second wiring in the second region being larger than the width thereof in the third region.

7. A semiconductor device according to claim 6, wherein the die pad is exposed to a surface opposite to a mounting surface of the sealing member.

8. A method of manufacturing a semiconductor device assembled by using a lead frame, comprising the steps of:

(a) providing a lead frame, the lead frame having a die pad smaller than a main surface of a semiconductor chip and a plurality of leads each comprising an outer terminal portion and an inner lead portion, the inner lead portions of the leads being bent in a direction away from a surface on which the outer lead portions of the leads are arranged;

(b) providing the semiconductor chip, the semiconductor chip having a semiconductor element and a plurality of electrodes;

(c) protruding the semiconductor chip from the die pad and bonding a back side of the semiconductor chip and the die pad with each other;

(d) connecting the electrodes of the semiconductor chip and corresponding said inner lead portions of the lead frame electrically with each other through bonding wires;

(e) sealing the semiconductor chip, the bonding wires and

the plural inner lead portions with resin to form a sealing member in such a manner that the outer terminal portions of the leads are exposed to a mounting surface of the sealing member and that the inner lead portions of the leads are disposed inside the sealing member; and

separating the plural leads from the lead frame.

9. A method according to claim 8, wherein, in the step (c), the semiconductor chip is disposed on the die pad while being chucked by an inverted pyramidal collet, and thereafter the semiconductor chip and the die pad are bonded together.

10. A method according to claim 9, wherein, in the inverted pyramidal collet, an angle between a contact surface of the collet which surface comes into contact with the semiconductor chip when the chip is chucked and an axis of the collet which axis is parallel to the vertical direction, is not larger than 45°.

11. A method according to claim 8, wherein the semiconductor chip provided in the step (b) comprises:

a first wiring formed on a semiconductor substrate and connected electrically to a ground potential;

a first insulating film formed on the first wiring; and

a second wiring formed on the first insulating film

and serving as a signal transmission line,

the second wiring including a first region, a second region, and a third region,

the second region of the second wiring being positioned between the first region and the third region,

with bonding wires being connected to the first region of the second wiring, and

the width of the second wiring in the second region being larger than the width thereof in the third region.

12. A method according to claim 11, wherein the area of the first region of the second wiring on the first wiring in the semiconductor chip is changed according to the length of each of the bonding wires to change an internal capacitance of the chip.

13. A method according to claim 11, wherein, in the semiconductor chip, output electrodes for a high-speed signal are arranged at positions opposed to input electrodes for a high-speed signal.

14. A method according to claim 8, wherein the sealing with resin is performed in such a manner that the die pad is exposed to a surface opposite to the mounting surface of the sealing member.

15. A method of manufacturing a semiconductor device assembled by using a lead frame, comprising the steps of:

(a) providing a lead frame, the lead frame having a die pad and a plurality of leads each comprising an outer terminal portion and an inner lead portion, the inner lead portions of the leads being bent in a direction away from a surface on which the outer terminal portions of the leads are arranged;

(b) providing a semiconductor chip having a semiconductor element and a plurality of electrodes;

(c) bonding a back side of the semiconductor chip and the die pad with each other;

(d) connecting the electrodes of the semiconductor chip and corresponding said inner lead portions of the lead frame electrically with each other through bonding wires;

(e) sealing the semiconductor chip, the bonding wires and the plural inner lead portions with resin to form a sealing member in such a manner that the outer terminal portions of the leads are exposed to a mounting surface of the sealing member and that the inner lead portions of the leads are disposed inside the sealing member; and

(f) separating the plural leads from the lead frame,

the semiconductor chip comprising:

a first wiring formed on a semiconductor substrate and connected electrically to a ground potential;

a first insulating film formed on the first wiring;

and

a second wiring formed on the first insulating film and serving as a signal transmission line,

the second wiring including a first region, a second region and a third region,

the second region of the second wiring being positioned between the first region and the third region,

with bonding wires being connected to the first region of the second wiring, and

the width of the second wiring in the second region being larger than the width thereof in the third region.

16. A method of manufacturing a semiconductor device assembled by using a lead frame, comprising the steps of:

(a) providing a lead frame, the lead frame having a die pad smaller than a main surface of a semiconductor chip and a plurality of leads each comprising an outer terminal portion and an inner lead portion, at least one of each said outer terminal portion and each said inner lead portion having a portion bent in a direction away from a surface on which the outer terminal portions are arranged;

(b) providing the semiconductor chip, the semiconductor chip having a semiconductor element and a plurality of electrodes;

(c) protruding the semiconductor chip from the die pad and

bonding a back side of the semiconductor chip and the die pad with each other;

(d) connecting the electrodes of the semiconductor chip and corresponding said inner lead portions of the lead frame electrically with each other through bonding wires;

(e) sealing the semiconductor chip, the bonding wires and the plural inner leads with resin to form a sealing member in such a manner that the outer terminal portions of the leads are exposed to the exterior from side faces of the sealing member and that the inner lead portions of the leads are disposed inside the sealing member; and

(f) separating the plural leads from the lead frame,

the semiconductor chip comprising:

a first wiring formed on a semiconductor substrate and connected electrically to a ground potential;

a first insulating film formed on the first wiring; and

a second wiring formed on the first insulating film and serving as a signal transmission line,

the second wiring including a first region, a second region and a third region,

the second region of the second wiring being positioned between the first region and the third region,

with bonding wires being connected to the first

region, and

the width of the second wiring in the second region being larger than the width thereof in the third region.

17. A method according to claim 16, wherein the sealing with resin is performed in such a manner that the die pad is exposed to a surface opposite to a mounting surface of the sealing member.